Amendments to the Specification:

Please replace paragraph **[0002]** of the substitute specification filed September 19, 2002 with the following amended paragraph:

[0002] State of the Art: Electrostatic discharge (hereinafter "ESD") and electrical overstress (hereinafter "EOS") are two common phenomenon that occur during human or mechanical handling of semiconductor integrated circuitry (hereinafter "IC") devices. The input pins to an IC device are highly sensitive to damage from the voltage spike of an ESD, which can reach potentials in excess of hundreds of volts. If a charge of this magnitude is brought into contact with a pin of an IC device, a large flow of current may surge through the IC device. Although this current surge may be of limited energy and duration, it can cause a breakdown of insulating barriers within the IC device (usually gate oxide insulating barriers of an MOS (metal-oxide-semiconductor) IC device). This breakdown of the insulating barriers within an IC device can result in permanent damage to the IC device and, once damaged, it is impossible to repair the IC device.

Please replace paragraph **[0056]** of the substitute specification filed September 19, 2002 with the following amended paragraph:

[0056] A deposition mask 152, such as TEOS, is patterned on the second barrier layer 128 having openings 154 over the contact plugs 148, as shown in FIG. 11. The deposition mask openings 154~~152~~ may be of any shape or configuration, including, but not limited to, circles, ovals, rectangles, or even long slots extending over several source regions 106 and drain regions ~~region~~ 108, respectively. A second conductive material 156, such as n-doped polysilicon, is deposited over the deposition mask 152 to fill the deposition mask openings 154, as shown in FIG. 12. The second conductive material 156 is planarized, as shown in FIG. 13, to electrically separate the second conductive material 156 within each deposition mask opening 154 (see FIG. 11). The planarization is preferably performed using a mechanical abrasion technique, such as a

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CMP process. The deposition mask 152 may be removed (optional) to leave the second conductive material forming contact lands 158 on a third intermediate structure 160, as shown in FIG. 14.

Please replace paragraph **[0061]** of the substitute specification filed September 19, 2002 with the following amended paragraph:

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[0061] FIG. 27 illustrates a top plan view of the source contact metallization 186 and the drain contact metallization 188. The source contact metallization 186 is in electrical communication with a source plate 194 and the drain contact metallization 188 is in contact with a drain input pad 192. The transistor gate members 112 are connected to a common electrical contact 196. The transistor gate ~~transistorgate~~ members 112 and the upper contacts 178 are illustrated for visual orientation, but it is understood that they would not be visible with a top plan view. FIG. 28 illustrates a schematic of the ESD/EOS protection structure between the drain input pad 192 and integrated circuitry 198 to be protected.